# STATIC TIMING MODEL FOR COMBINATORIAL GATES HAVING CLOCK SIGNAL INPUT

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## ABSTRACT OF THE DISCLOSURE

A method of modeling a combinatorial gate which includes providing a data signal input at the combinatorial gate, providing a clock signal input at the combinatorial gate, propagating the clock signal as an output signal when the output of the combinatorial gate corresponds to the clock signal, and propagating the data signal as an output when the output of the combinatorial gate corresponds to the data signal, the propagating the data signal modeling a near domino function.